Claim 27. (Previously Added) The surface laminar circuit board of claim 25, wherein said dielectric layer has a thickness, in a region over said conductive material, equal to or less than about 40 micrometers.

Claim 28. (Previously Added) The surface laminar circuit board of claim 25, wherein all of said conductive pad is disposed over the portion of said insulating layer exposed by the hole.

Claim 29. (Previously Added) The surface laminar circuit board of claim 23, wherein all of said conductive pad is disposed over the portion of said insulating layer exposed by the hole.

REMARKS

The Examiner's Action mailed on December 4, 2002 has been received and its contents carefully considered.

In this Amendment, Applicants have amended claims 1, 6, 7, 20, and 25. It is noted that the changes to these claims have not been made to help distinguish over the art of record, nor in an attempt to further define or limit the claims in any manner. Instead, and since the Examiner had apparently found various terms in the claims to be confusing, claims 1 and 20 have been amended to change the term "majority" to its dictionary definition of --over 50%--. Claims 6, 7, 20 and 25 have been amended to

change the term "signal ground" to simply --ground--, in accordance with the Examiner's gracious suggestion. It was not believed that the use of these original terms rendered the claims indefinite, as alleged by the Examiner's Action. However, since the scope of the claims remains the same, the claims have been amended in the manner described in order to facilitate the prosecution of this application.

Claims 1, 20 and 23 are the independent claims, and claims 1-12 and 20-29 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claims 1-3, 5-12 and 20-21 as being indefinite. In particular, the Examiner states that independent claims 1 and 20 are indefinite for being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections.

In the Examiner's Response to Arguments, the Examiner clarifies the rejection by stating that rejection is not being made because of any missing element, but because the relationship between the elements is unclear.

The Examiner relies on MPEP § 2172.01 in support of this rejection. This section of the MPEP discusses omitted subject matter from a claim that is disclosed to be essential to the invention. Further, this section of the MPEP states that such a claim may be rejected under 35 USC § 112, first paragraph. However, the Examiner's Action has not rejected these claims under the first paragraph, but under the second paragraph of 35 USC § 112. Further, and as noted above, the Examiner's Action has explicitly stated that there are no essential elements missing from the claims. Thus, the Examiner's reliance on MPEP § 2172.01 appears to be misplaced

Moreover, it is submitted that the claims are definite within the purview of 35 USC § 112, since the claims do particularly point out and distinctly claim the subject matter of the invention. In particular, and in contrast to the allegation presented by the Examiner's Action, independent claims 1 and 20 do provide a positional relationship between the conductive pad, the hole, the insulating layer and the conductive layer. That is, claims 1 and 20 recite that an outer periphery of the hole defines an area, and that over 50% of the conductive pad is in that area. These claims also recite that the hole is formed in a conductive layer, which is disposed on an insulating layer. No further recitation regarding the positional relationships is believed to be necessary. Further, there is no requirement from Section 112, second paragraph, that the exact structural cooperative relationships, as requested by the Examiner, be provided.

It is further noted that the Examiner's Action states that the "claims by themselves need to be clear enough to completely describe the invention". However, there is no requirement from Section 112, second paragraph, that the claims must completely describe the invention, as asserted by the Examiner's Action. Instead, this section of Section 112 only requires that the claims particularly point out and distinctly claim the subject matter that the applicant regards as his invention. As noted, Applicants' claims fulfill this requirement.

It is further noted that claims 1 and 20 offer sufficient breadth to read upon all of the disclosed embodiments of Applicants' invention. However, simply because Applicants' claims are sufficiently broad to read upon more than one embodiment does not render the claims indefinite. The MPEP §2173.04 specifically states that the breadth of a claim is not to be equated with indefiniteness. As such, since the claims do

particularly point out and distinctly claim the subject matter of the invention, it is submitted that the claims are definite within the purview of 35 USC § 112, second paragraph.

Furthermore, the Examiner has also rejected the claims since the term "a majority thereof within an area defined by an outer periphery of the hole" is allegedly vague. It is believed that the basis for this rejection is the use of the term "majority", which term is believed to be definite within the purview of 35 USC Section 112, second paragraph. Nevertheless, and only in order to facilitate the prosecution of the application, Applicants have amended claims 1 and 20 to change the term "majority" to --over 50%--.

Moreover, regarding claims 6, 20 and 25, the Examiner has stated that it is not clear if the conductive layer is a signal layer, or a ground layer that is close to a signal layer. Although it is believed that the claims are definite within the purview of 35 USC Section 112, second paragraph, and only in order to facilitate the prosecution of the application, Applicants have amended these claims (as well as claim 7) in the manner suggested by the Examiner.

It is submitted that the claims are definite within the purview of 35 USC § 112, second paragraph, and it is thus requested that these rejections be withdrawn.

The Examiner has rejected claims 1, 6-8 and 12 as being anticipated by *McMahon* (USP 6,075,712). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 USC § 102, only if <u>all</u> the features and <u>all</u> the relationships recited in the claim are

taught by the reference structure either by clear disclosure or under the principle of inherency. Further, anticipation requires that the identical invention be already known by others, that is, the claimed invention is not new (*see Minnesota Mining & Mfg. Co. v Johnson & Johnson Orthopedics, Inc.* . . . (Fed. Cir. 1992)).

Applicants' independent claim 1 is directed to a surface laminar circuit board that includes, *inter alia*, an insulating layer, and a conductive layer disposed on an upper surface of the insulating layer. The conductive layer has a hole therein. A conductive pad is provided that is for receiving a surface mounted component thereon.

McMahon discloses a flip chip 202 which can be mounted on a package substrate 250, as shown in Figures 5A and 5B. Chip 202 includes a semiconductor substrate 204 having circuit elements 206 formed in a front surface thereof. Chip 202 also includes a conductor region 210, which includes multiple layers of conductive lines 208, 209. Conductive lines 208, 209 are connected to the circuit elements 206 using conductive vias 212. Contact pads 218 are connected to the conductive lines 208, 209 through vias 216. Further, an on-chip cache memory device 560 is located within a recess of the semiconductor substrate 204, and is connected to the conductive lines 208, 209 using vias 540.

However, and in contrast to the present invention, the cited reference does not disclose (or even suggest) a surface laminar circuit board, as recited in claim 1, and as alleged by the Examiner's Action. Instead, the cited reference is directed to a flip chip. It is unclear how the Examiner's Action can equate a flip chip as being a surface laminar circuit board; however, one skilled in the art would realize the differences between these two distinct devices.

The Examiner's Action has also held that the space between adjacent conductors 208, 209 constitutes a hole, as recited in claim 1. However, it is respectfully submitted that there is no disclosure from this reference to support this assertion. Instead, the cited reference discloses that the "conductors" 208, 209 are conductive lines. Any space formed between adjacent lines is thus simply that: a space. However, there is no disclosure from this reference that these spaces are actually holes formed in a conductive layer. Further, Applicants are not aware of any interpretation that would render a space between two adjacent lines to be equivalent to a hole formed in a layer. Moreover, in order to read upon this portion of Applicants' claim, at least one of these conductive lines would need to have a hole formed therein. However, there is no disclosure of such a feature.

Further, the cited reference does not disclose or suggest a conductive pad having a majority (i.e., over 50%) thereof within an area defined by an outer periphery of a hole. As noted above, the cited reference does not disclose a hole. Thus, the cited reference cannot possibly disclose the positional relationship of a conductive pad to a hole.

Moreover, claim 1 recites that the conductive pad is for receiving a surface mounted component thereon. The Examiner's Action has equated circuit elements 206 as being conductive pads, and the on-chip cache memory device 560 as being a surface mounted component. However, the circuit elements 206 are deeply embedded within the chip 202, and thus are not in a position to have a surface mounted component received or mounted thereon. In fact, the on-chip cache memory device 560 is not received on the circuit elements 206, but is instead received on contacts 544.

Further, it is respectfully submitted that on-chip cache memory device 560 is not a surface mounted component, as the term is known to those skilled in the art. A brief description of surface mounted components is provided in Applicants' specification, on page 2, line 16 through page 3, line 7.

As such, it is submitted that the Examiner has failed to establish a *prima facie* case of anticipation against Applicants' independent claim 1.

Moreover, dependent claims 6-8 and 12 are submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein. As such, it is requested that these claims be allowed and it is further requested that this rejection be withdrawn.

The Examiner has further rejected claims 2, 3, 9-11, 20 and 21 as being obvious over *McMahon* in view of *Trask et al.* (USP 5,034,091) . It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

As noted above, Applicants' independent claim 1 is *prima facie* patentably distinguishable over *McMahon*. Further, *Trask et al.* do not overcome the deficiencies of *McMahon*. As such, dependent claims 2, 3 and 9-11 are submitted to be patentably distinguishable over the cited references for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recite therein.

Moreover, independent claim 20 and dependent claim 21 are submitted to be patentably distinguishable over the cited references for at least the following reasons.

Applicants' independent claim 20 is directed to a surface laminar circuit board that includes, *inter alia*, an insulating layer, and a ground conductive layer disposed on an upper surface of the insulating layer. The ground conductive layer has a hole therein. A conductive pad is provided that is for receiving a surface mounted component thereon. The surface mounted component is mounted on the conductive pad.

The Examiner's Action relies on the embodiment shown in Figure 2b for this rejection. In this embodiment, *McMahon* discloses a flip chip 202 which can be mounted on a package substrate 250. Chip 202 includes a semiconductor substrate 204 having circuit elements 206 formed in a front surface 214 thereof. Chip 202 also includes traces 260 on the front surface 214 of the substrate 204. Traces 260 are coupled to the circuit elements 206 using further traces 262 and vias 264. The Examiner is apparently taking the position that the lower portion of the chip 202, i.e., the conductor region 210, constitutes a surface laminar circuit board, and the upper portion of the chip, i.e., the substrate 204, constitutes a surface mounted component.

However, and in contrast to the present invention, the cited reference does not disclose or suggest a surface laminar circuit board, as recited in claim 20, and as asserted by the Examiner's Action. Instead, the cited reference is directed to a flip chip. It is unclear how the Examiner's Action can equate a flip chip, especially the conductor region 210 of the chip, as being a surface laminar circuit board; however, one skilled in the art would realize the structural and functional differences between these two distinct devices.

The Examiner's Action has also held that the space between adjacent traces 262 constitutes a hole, as recited in claim 20. However, it is respectfully submitted that there is no disclosure from this reference to support this assertion. In fact, the cited reference is entirely silent as to the configuration of the traces 262. However, it is respectfully submitted that any space between adjacent ones of the traces 262 is simply that: a space. There is no disclosure or suggestion from this reference that these spaces are actually holes formed in a conductive layer. Further, Applicants are not aware of any interpretation that would render a space between two adjacent traces to be equivalent to a hole formed in a layer. Moreover, in order to read upon this portion of Applicants' claims, at least one of these traces would need to have a hole formed therein. However, there is no disclosure or teaching of such a feature.

Further, the cited reference does not disclose or suggest a conductive pad having a majority (i.e., over 50%) thereof within an area defined by an outer periphery of a hole. As noted above, the cited reference does not disclose a hole. Thus, the cited reference cannot possibly disclose the positional relationship of a conductive pad to a hole.

Moreover, claim 20 recites that the conductive pad is for receiving a surface mounted component thereon. The Examiner's Action has equated circuit elements 206 as being conductive pads, and the entire substrate 204 of the chip 202 as being a surface mounted component. However, the circuit elements 206 are deeply embedded within the chip 202, and thus are not in a position to have a surface mounted component received or mounted thereon. Moreover, the cited reference explicitly discloses that the circuit elements 206 form a part of the substrate 204, and that the

elements 206 are formed in substrate 204 (see column 2, lines 40-42). Thus, even assuming *arguendo* that the conductor region 210 could be construed as being a surface laminar circuit board, as presented by the Examiner's Action, such "circuit board" would not include the conductive pads, since the "conductive pads" 206 are part of the "surface mounted component" 204. Further, it is respectfully submitted that the semiconductor substrate 204 is not a surface mounted component, as the term is known to those skilled in the art. A brief description of surface mounted components is provided in Applicants' specification, on page 2, line 16 through page 3, line 7.

The Examiner's Action acknowledges that *McMahon* does not teach a photosensitive dielectric layer, or a photo micro-via. The Examiner's Action thus relies on *Trask et al.* as teaching a photosensitive dielectric layer, and a photo micro-via. However, *Trask et al.* do not overcome the many other deficiencies of *McMahon.* As such, it is submitted that the Examiner has failed to establish a *prima facie* case of obviousness against Applicants' independent claim 20 and dependent claim 21. It is thus requested that these rejections be withdrawn, and it is further requested that these claims be allowed.

The Examiner has further rejected claim 5 as being obvious over *McMahon* in view of *Trask et al.*, and further in view of *Higgins, Jr.* (USP 5,039,965) . It is submitted that this claim is patentably distinguishable over the cited references for at least the following reasons.

As noted above, the combination of *McMahon* and *Trask et al.* fail to render Applicants' claim 1 obvious. Moreover, *Higgins, Jr.* fails to overcome the above-noted deficiencies of *McMahon* and *Trask et al.* As such, it is submitted that claim 5 is

patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which this claim depends, as well as for the additional features recited therein. It is thus requested that this rejection be withdrawn, and it is further requested that this claim be allowed.

The Examiner has further rejected claims 23-29 as being obvious over *McMahon* in view of *Snodgrass et al.* (USP 5,311,406). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Claim 23 is directed to a surface laminar circuit board that includes, *inter alia*, an insulating layer, and a sheet of conductive material disposed on an upper surface of the insulating layer. The sheet of conductive material has a hole therein. A conductive pad is provided that is for receiving a surface mounted component thereon.

Similar to the rejection against claim 20, the Examiner's Action relies on the embodiment shown in Figure 2b of *McMahon* for this rejection. However, and as previously noted, the cited reference does not disclose or suggest a surface laminar circuit board, as recited in claim 23, and as asserted by the Examiner's Action. Instead, the cited reference is directed to a flip chip.

The Examiner's Action has also asserted that the space between adjacent traces 262 constitutes a hole, as recited in claim 23. However, and again as previously noted, there is no disclosure from this reference to support the Examiner's assertion. In fact, the cited reference is entirely silent as to the configuration of the traces 262. However, it is respectfully submitted that the space between adjacent ones of the traces 262 is simply that: a space. There is no disclosure or suggestion from this reference that these spaces are actually holes formed in a conductive layer. Further, Applicants are

not aware of any interpretation that would render a space between two adjacent traces to be equivalent to a hole formed in a layer. Moreover, in order to read upon this portion of Applicants' claims, at least one of these traces would need to have a hole formed therein. However, there is no disclosure of such a feature.

Further, the cited reference does not disclose or suggest a conductive pad having a major portion thereof disposed directly over a portion of the insulating layer exposed by the hole. As noted above, the cited reference does not disclose a hole. Thus, the cited reference cannot possibly disclose or suggest the positional relationship of a conductive pad to a hole.

Moreover, claim 23 recites that the conductive pad is for receiving a surface mounted component thereon. The Examiner's Action has equated circuit elements 206 as being conductive pads, and the entire substrate 204 of the chip 202 as being a surface mounted component. However, the circuit elements 206 are deeply embedded within the chip 202, and thus are not in a position to have a surface mounted component received or mounted thereon. Moreover, the cited reference explicitly discloses that the circuit elements 206 form a part of the substrate 204, and that the elements 206 are formed in substrate 204 (see column 2, lines 40-42). Thus, even assuming *arguendo* that the conductor region 210 could be construed as being a surface laminar circuit board, as presented by the Examiner's Action, such "circuit board" would not include the conductive pads, since the "conductive pads" 206 are part of the "surface mounted component" 204. Further, it is respectfully submitted that the semiconductor substrate 204 is not a surface mounted component, as the term is known to those skilled in the art. As previously noted, a brief description of surface

mounted components is provided in Applicants' specification, on page 2, line 16 through page 3, line 7.

The Examiner's Action acknowledges that *McMahon* does not teach a conductive material being in the form of a sheet, or a hole exposing a portion of the insulating layer, or the sheet of conductive material completely surrounding an area defined by the hole, with the area being in registration with, and corresponding in shape and size to the portion of the insulating layer exposed by the hole.

The Examiner's Action thus relies on the teachings of *Snodgrass et al.* as teaching these features. *Snodgrass et al.* disclose a wiring board having a metallic layer 10, a dielectric layer 20, a metallic sheet 30, a first fiberglass sheet 40, a metallic layer 50, a second fiberglass layer 60, and a metallic layer 70, disposed one on top of the other in the order given. Layer 30 is a copper sheet, and serves as a ground plane for the circuit elements of layer 10. Further, vias (not shown) are formed to connect layer 10 to the transmission lines of layer 50.

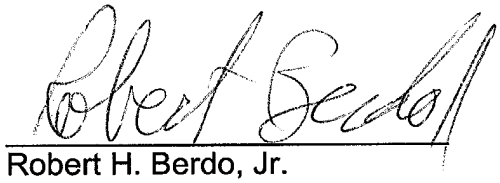
However, *Snodgrass et al.* do not overcome the above-noted deficiencies of *McMahon.* Moreover, and in contrast to the assertion presented by the Examiner's Action, this reference does not disclose or suggest "a hole located over an insulating layer exposing a portion of it". Although this reference does disclose forming vias, the specific positioning of the vias is not provided. However, since the vias interconnect the layer 10 with the layer 50, it can be assumed that the vias pass through the layers 20, 30, and 40, and are disposed under layer 10 and over layer 50. Thus, any hole formed in the conductive sheet 30 by such vias would not expose a portion of an insulating layer over which they are disposed, as alleged by the Examiner's Action. That is, the

vias would only be disposed over the fiberglass layer 60, i.e., they would pass through the other insulating layers. However, the vias would not expose the fiberglass layer 60, since there would be a metallic layer 50 therebetween. As such, it is submitted that the Examiner has failed to establish a *prima facie* case of obviousness against Applicants' independent claim 23 and dependent claims 24-29. It is thus requested that these rejections be withdrawn, and it is further requested that these claims be allowed.

It is submitted that this application is in condition for allowance. Such action, and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



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Date

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